

Application No. 10/724,028  
Amendment dated November 15, 2005  
After Final Office Action of October 26, 2005

Docket No.: 08211/0200253-US0 (P05742)

-2-

**AMENDMENTS TO THE CLAIMS**

1. (Previously Presented) A circuit comprising:  
a first transistor;  
a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor, as a telescopic cascode arrangement; and  
a keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.
- 2-5. (Canceled)
6. (Previously Presented) The circuit of Claim 1, wherein  
the keeper switch circuit comprises a keeper transistor including:  
a gate that is coupled to the drain of the second transistor;  
a source that is coupled to one of a group consisting of the source of the second transistor and the gate of the second transistor; and  
a drain that is coupled to the other of the group consisting of the source of the second transistor and the gate of the second transistor.
7. (Canceled)
8. (Previously Presented) The circuit of Claim 6, wherein  
the second transistor is one of a group consisting of an n-type transistor and the p-type transistor, and the keeper transistor is the other of the group consisting of the n-type transistor and the p-type transistor.
9. (Canceled)
10. (Canceled)

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Application No. 10/724,028

Docket No.: 08211/0200253-US0 (P05742)

Amendment dated November 15, 2005

-3-

After Final Office Action of October 26, 2005

11. (Original) A logic circuit comprising:  
a first transistor;  
a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor, wherein the second transistor includes:  
a gate that is coupled to a bias node,  
a drain that is coupled to a first output node, and  
a source that is coupled to a second output node;  
a third transistor;  
a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor, wherein the fourth transistor includes:  
a gate that is coupled to the bias node,  
a drain that is coupled to a first complement output node, and  
a source that is coupled to a second complement output node,  
a first keeper switch circuit that is coupled to the bias node, the second complement output node, and the second output node, and  
a second keeper switch circuit that is coupled to the bias node, second output node, and the second complement output node.

12. (Original) The logic circuit of Claim 11, wherein  
the second transistor is configured to receive a first cascode bias voltage at the bias node, wherein  
the first cascode bias voltage is suitable for biasing a cascode transistor.

13. (Original) The logic circuit of Claim 11, wherein  
the first keeper switch circuit is configured to influence a resistance between the second output node and the bias node in response to a control signal.

14. (Original) The logic circuit of Claim 11, wherein  
the first keeper switch circuit is configured to:

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Application No. 10/724,028  
Amendment dated November 15, 2005  
After Final Office Action of October 26, 2005

Docket No.: 08211/0200253-US0 (P05742)

-4-

receive a control signal at the second complement output node;  
couple the second output node to the bias node if the control signal  
corresponds to a first logic level; and  
isolate the second output node from the bias node if the control signal  
corresponds to a second logic level.

15. (Original) The logic circuit of Claim 11, wherein  
the logic circuit is arranged to operate as a level shifter circuit.

16. (Previously Presented) The logic circuit of Claim 11, wherein  
the first keeper switch circuit comprises a keeper transistor including:  
a gate that is coupled to the second complement output node,  
a source that is coupled to one of a group consisting of the second output  
node and the bias node, and  
a drain that is coupled to the other of the group consisting of the second  
output node and the bias node.

17. (Previously Presented) The logic circuit of Claim 16, wherein  
the second transistor is one of a group consisting of an n-type transistor and a p-type  
transistor, and the keeper transistor is the other of the group consisting of the n-type transistor and  
the p-type transistor.

18. (Previously Presented) The logic circuit of Claim 11, wherein  
the second keeper switch circuit comprises a fifth transistor including:  
a gate that is coupled to the second output node,  
a source that is coupled to one of a group consisting of the second  
complement output node and the bias node, and  
a drain that is coupled to the other of the group consisting of the second  
complement output node and the bias node.

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Application No. 10/724,028  
Amendment dated November 15, 2005  
After Final Office Action of October 26, 2005

Docket No.: 08211/0200253-US0 (P05742)

-5-

19. (Previously Presented) The logic circuit as in Claim 18, wherein the first keeper switch circuit comprises a keeper transistor, and wherein the second transistor is one of a group consisting of an n-type transistor and a p-type transistor, the keeper transistor is the other of the group consisting of the n-type transistor and the p-type transistor, and the fifth transistor is the other of the n-type transistor and the p-type transistor.

20. (Canceled)

21. (Canceled)

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